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CMOS-RC Colpitts Oscillator Design Using Floating Fractional-Order Inductance Simulator

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***Abstract*—This paper deals with CMOS fractional-order inductance (FoL) simulator design and its utilization in 2.75th-order Colpitts oscillator providing high frequency of oscillation. The proposed floating FoL is composed of two unity-gain current followers (CF±s), two inverting voltage buffers, a transconductor, and a fractional-order capacitor (FoC) of order 0.75, while the input intrinsic resistance of CF± is used as design parameter instead of passive resistor. The resulting equivalent inductance value of the FoL can be adjusted via order of FoC, which was emulated via 5th-order Foster II RC network and values optimized using modified least squares quadratic method. In frequency range 138 kHz – 2.45 MHz the L_γ shows ±5 degree phase angle deviation. Theoretical results are verified by SPICE simulations using TSMC 0.18 µm level-7 LO EPI SCN018 CMOS process parameters with ±1 V supply voltages.**

Keywords—Colpitts oscillator; fractional-order capacitor; FoC; fractional-order inductor; FoL; fractional-order oscillator

I. INTRODUCTION

At present, the number of applications of fractional calculus rapidly grows. It is due to the fact that this powerful mathematical tool allows us to describe and model a real-world phenomenon more accurately than via classical "integer" methods. In general, most of the real-world phenomena are of fractional origin, however, for many of them the fractionality is insignificant. Typical issues solved in fractional-order domain are the voltage-current relation of a semi-infinite lossy transmission line [1], oscillation of the linear/non-linear system, where the oscillation gives the ideal response [2], impedance response of the tissues especially in bioengineering [3], robustness of the systems in control theory [4], synchronization of nonlinear fractional-order chaotic systems [5], and many others [6] (and references cited therein). Unless integer-order inductors or their emulators [6], fractional-order ones are not commercially available and need to be emulated through active building blocks [7], [8] or resistor-inductor networks [9]. Two most popular high-frequency oscillators employing inductors are the Colpitts and Hartley oscillators [10], [11] and both were investigated under some of the following design conditions in integer-order cases: (i) power consumption, (ii) supply voltage, (iii) transistor current density, (iv) sizing (area, aspect ratio, finger width), (v) inductance, (vi) quality factor, and (vii) considering the full models of the transistors available within the process design kit. However, in open literature, recently few studies are reported on fractional-order Hartley oscillator [12], while there is no available fractional-order Colpitts oscillator at present. The mathematical definitions of the fractional-order oscillation criteria are known and already investigated [13]. The implementation of such oscillators evidently require the use of a fractional-order capacitor (FoC), which brings to researchers several design features such as possibility of changing the frequency of oscillation (FO) and condition of oscillation (CO). Therefore, this study aims to investigate the fractional-order case of Colpitts oscillator employing a compact CMOS fractional-order inductance (FoL) simulator, in which the FoC with $12\ \mathrm{nF}\cdot\mathrm{s}^{-0.25}$ value is emulated via 5th-order Foster II RC network. The behavior of proposed FoL and Colpitts oscillator was verified by SPICE simulations.

II. A FRACTIONAL-ORDER COLPITTS OSCILLATOR

A. Introduction of the General Fractional Case

The Colpitts oscillator is an LC oscillator, which contains a tuned tank circuit consisting of one inductor and two capacitors; the two capacitors therein are making a capacitive voltage divider. Colpitts oscillator implemented using two CMOS-based transconductors is shown in Fig. 1, wherein the three terminal LC networks are connected in such a manner that between two nodes of the three terminal LC circuits, a transconductor of gain $-g_m$ is connected, whereas the common node of the two capacitors is connected to ground [14]. Replacing the ideal capacitors C_i for $i = \{\alpha, \beta\}$ with FoCs (i.e. C_α and C_β) having impedance $Z_\alpha(s) = 1/(s^\alpha C_\alpha)$,

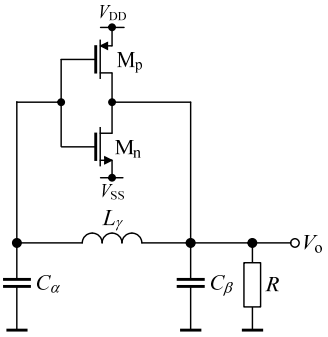

Fig. 1. Voltage-mode Colpitts oscillator.

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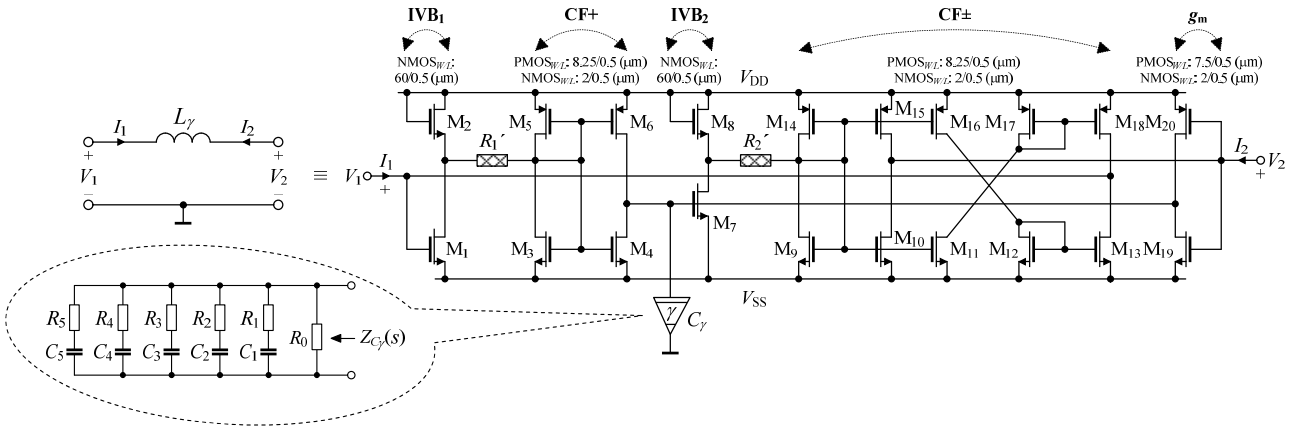


Fig. 2. Proposed CMOS fractional-order inductance simulator including RC network emulating fractional-order capacitor.

$Z_\beta(s) = 1/(s^\beta C_\beta)$, and FoL ($L_\gamma$) with impedance of $Z_\gamma(s) = s^\gamma L_\gamma$, routine circuit analysis provides the following description of this fractional-order system [13]:

$$\begin{pmatrix} d^\alpha V_{C_\alpha}/dt^\alpha \\ d^\beta V_{C_\beta}/dt^\beta \\ d^\gamma I_{L_\gamma}/dt^\gamma \end{pmatrix} = \begin{pmatrix} 0 & 0 & 1/C_\alpha \\ -g_\mathrm{m}/C_\beta & -1/RC_\beta & -1/C_\beta \\ -1/L_\gamma & 1/L_\gamma & 0 \end{pmatrix} \begin{pmatrix} V_{C_\alpha} \\ V_{C_\beta} \\ I_{L_\gamma} \end{pmatrix}. \quad (1)$$

Hence, the characteristic equation (CE) from (1) has the following general form:

$$\mathrm{CE}: \quad s^{\alpha+\beta+\gamma} RC_\alpha C_\beta L_\gamma + s^{\alpha+\gamma} C_\alpha L_\gamma + s^\alpha RC_\alpha + s^\beta RC_\beta + Rg_\mathrm{m} + 1 = 0. \quad (2)$$

An ideal third-order Colpitts oscillator corresponds to setting $\alpha = \beta = \gamma = 1$, which results in the well-known CO: $g_\mathrm{m}R = C_1/C_2$ and FO: $\omega = \sqrt{1/(LC_{eff})}$, where $C_\mathrm{eff} = C_1C_2/(C_1+C_2)$ and it can be proved from (1) and (2).

B. Fractional-Order Inductor Case

Considering C_1 and C_2 as integer-order capacitors (i.e. $C_\alpha \Rightarrow C_1$ and $C_\beta \Rightarrow C_2$) and inductor L_γ remains as a fractional-order inductor, the general CE in (2) turns to:

$$\mathrm{CE}_\gamma: s^{2+\gamma} RC_1C_2L_\gamma + s^{1+\gamma} C_1L_\gamma + sR(C_1+C_2) + Rg_\mathrm{m} + 1 = 0, \quad (3)$$

and substituting $s = j\omega$ therein, the derived CO_γ and FO_γ are respectively given by:

$$\mathrm{CO}_\gamma: R = -\frac{1+\omega^{1+\gamma} C_1L_\gamma \cos\left[0.5\pi(1+\gamma)\right]}{\omega^{2+\gamma} C_1C_2L_\gamma \cos\left[0.5\pi(2+\gamma)\right] + g_\mathrm{m}} = -\frac{\omega^{1+\gamma} C_1L_\gamma \sin\left[0.5\pi(1+\gamma)\right]}{\omega^{2+\gamma} C_1C_2L_\gamma \sin\left[0.5\pi(2+\gamma)\right] + \omega(C_1+C_2)}, \quad (4)$$

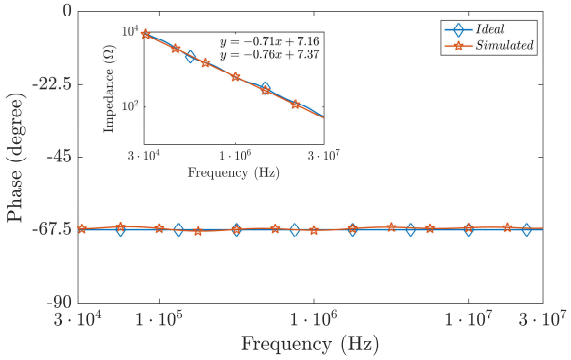
$$\begin{aligned} \mathrm{FO}_\gamma: \; & \omega^{2+\gamma} C_1^2C_2L_\gamma^2 - \omega C_1C_2L_\gamma \sin(0.5\pi\gamma) - \\ & - \omega C_1L_\gamma(C_1+C_2)\cos(0.5\pi\gamma) + \\ & + \omega^{-1} C_1L_\gamma g_\mathrm{m} \sin(0.5\pi\gamma) - \omega^{-\gamma}(C_1+C_2) = 0. \end{aligned} \quad (5)$$

As it is evident, the proposed oscillator offers independent tuning of the frequency and condition of oscillation.

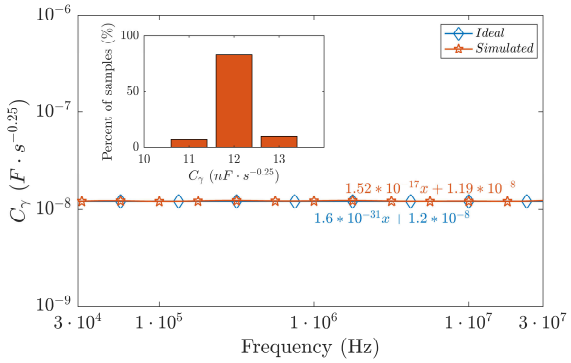
III. Realization of Proposed Circuits

In analog electronics, due to the large silicon area, cost, and lack of electronically tunability, CMOS-based inductance simulators are used [15]. The CMOS implementation of the proposed FoL simulator is shown in Fig. 2. It consists from two inverting voltage buffers (IVBs), two unity-gain current followers (CFs), and one simple transconductor. In brief, for example IVB_1 assuming that both NMOS work in saturation region, $V_\mathrm{THN1} = V_\mathrm{THN2}$, $+V_\mathrm{DD} = -V_\mathrm{SS}$, and process transconductance parameters $k_\mathrm{N1} = k_\mathrm{N2}$, voltage transfer can be described simply as $V_\mathrm{out} = -V_\mathrm{in}$. Thus, it behaves as a linear IVB without DC offset. In order to keep the M_1 in saturation region the condition $V_\mathrm{in} < V_\mathrm{out} + V_\mathrm{THN1}$ should be satisfied. Note that the M_2 always operates in saturation region since its drain and gate terminals are connected. Considering CF± structures used in Fig. 2, it can be observed that both were designed by superposition of top PMOS sourcing mirrors and bottom NMOS sinking mirrors. However, from another viewpoint this configuration may be seen as a cascade of two CMOS inverters with the first one having shorted input and output. In general, CF± can be described as $V_\mathrm{in} = R_{\mathrm{CF\_in}k} I_\mathrm{in}$ and $I_{\mathrm{out}\pm} = \pm I_\mathrm{in}$ for $k = \{1, 2\}$. Here, $R_{\mathrm{CF\_in}k}$ denotes intrinsic input resistance, which can be set via supply voltages. Finally, the current-voltage relationship of used transconductor is $I_\mathrm{out} = -g_\mathrm{m}V_\mathrm{in}$. Detailed description of used active building blocks (ABBs) can be find in [16], while transistors main parameters obtained after re-design are listed in Table I.

Considering described ABBs, one capacitor, and assuming matching condition $g_\mathrm{m} = 1/R_{\mathrm{CF\_in}1}$, while $R_{\mathrm{CF\_in}k} \approx R_k'$, routine circuit analysis yields the following short circuit admittance matrix $[Y_{L_\gamma}] = \frac{1}{s^\gamma L_\gamma}\begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}$, from which $L_\gamma = R_1'R_2'C_\gamma$. As it can be seen the equivalent inductance value is adjustable by order of the FoC (or phase). The Foster II structure has been used to realize the FoC with a fractional-order of $\gamma = 0.75$. Component values obtained via modified least squares quadratic (MLSQ) method. Parameters of both $C_{0.75}$ and subsequently $L_{0.75}$ emulators are summarized in Table II.



(a)



(b)

Fig. 3. Ideal and simulated (a) phase and (b) pseudo-capacitance responses of 0.75-order fractional-order capacitor.

IV. Simulation Results

The behavior of the ABBs used in CMOS implementation of the FoL simulator and subsequently in Colpitts oscillator in Figs. 1 and 2 have been verified by SPICE simulations with DC power supply voltages $+V_{DD} = -V_{SS} = 1$ V. In the design, transistors are modeled by the TSMC 0.18 µm level-7 LO EPI SCN018 CMOS process parameters ($V_{THN} = 0.3725$ V, $\mu_N = 259.5304$ cm^2/(V·s), $V_{THP} = -0.3948$ V, $\mu_P = 109.9762$ cm^2/(V·s), $T_{OX} = 4.1$ nm) [17]. The aspect ratios of transistors in structures and their main parameters obtained with AC and DC analyses are listed in Table I. The equivalent intrinsic input resistance and the transconductance gain value are set $g_m \cong (1/R_k' + 1/R_{IVB\_out}) \cong 835$ µA/V in order to fulfill the required parameter matching.

In order to verify the workability of the proposed Colpitts oscillator employing FoL simulator shown in Fig. 2, first of all the phase and pseudo-capacitance response of the FoC with an order $\gamma = 0.75$ and value $C_\gamma = 12$ nF·s$^{-0.25}$ (300 pF @ 407.5 kHz), emulated via 5th-order Foster II RC network, which has an admittance in following form: $Y_{C_\gamma} = 1/Z_{C_\gamma} = 1/R_0 + \sum_{k=1}^{5} sC_k/[sR_kC_k + 1]$ and values optimized using MLSQ method, has to be evaluated. Fig. 3(a) shows that the constant phase zone of the FoC is from 30 kHz to 30 MHz with –67.5 degrees, which is proven by the fitting equations as an inset of the figure. To estimate the equivalent order γ (or phase), the magnitude data simulated are fitted to the function $\log Z = \gamma \log f + \log(2\pi j)^\gamma C_\gamma$. Similarly, the pseudo-capacitance with stable C_γ is shown in Fig. 3(b). Note that the phase angle deviation in given range is only ±0.9 degree, while the corresponding relative pseudo-capacitance error in same range varies from –1.35% to +0.6%.

The performance of the proposed FoL simulator shown in Fig. 2 was also evaluated. Fig. 4 shows the effect of C_γ vs. γ on FoL magnitude. The simulated phase (pseudo)-inductance responses of 0.75 and integer-order inductance simulator are shown in Fig. 5. In this case the circuit was simulated with C and C_γ given above, which in fractional-order case theoretically resulted in $L_{\gamma\_theor} = 17.3$ mH·s$^{-0.25}$ and the simulated one has a value $L_{\gamma\_sim} = 18.4$ mH·s$^{-0.25}$. Considering ±5 degree deviation in phase, the useful frequency range for $L_{0.75}$ is about 138 kHz up to 2.45 MHz. Both 2.75th and 3rd-

TABLE I. Behavior of CMOS Transconductor, IVB, and CF±.

Transconductor (g_m)	
Parameter	***Value***
Transconductance gain g_m I_{out}/V_{in} (µA/V)	835
Tracking error ε_{gm} @ g_o = 833 µA/V (–)	–0.002
$f_{-3\ dB}$ @ g_m (GHz)	7.195
DC linearity for V_{in} (V)	±0.535
$R_{gm\ in}$ (Ω)	≅ ∞
$R_{gm\ out}$ (kΩ) ‖ $C_{gm\ out}$ (fF)	64.44 ‖ 6.42
Inverting Voltage Buffer (IVB)	
Parameter	***Value***
Voltage gain V_{out}/V_{in} gain (β_o)	0.972
Tracking error $\varepsilon_{\beta o}$ (–)	0.028
$f_{-3\ dB}$ @ V_{out}/V_{in} (GHz)	17.152
DC linearity V_{out}/V_{in} (V)	–1 → +0.445
$R_{IVB\ in}$ (Ω)	≅ ∞
$R_{IVB\ out}$ (Ω)	80.6
Current Follower (CF±)	
Parameter	***Value***
Current gains I_{out+}/I_{in}; I_{out-}/I_{in} (α_{oj})	0.982; 0.947
Tracking errors $\varepsilon_{\alpha oj}$ (–)	0.018; 0.053
$f_{-3\ dB}$ @ I_{out+}/I_{in}; I_{out-}/I_{in} (GHz)	1.138; 0.871
DC linearity I_{out+}/I_{in}; I_{out-}/I_{in} (µA)	±944; ±333
$R_{CF\ in}$ (R_k') (kΩ)	1.122
$R_{CF\ out+}$ (kΩ) ‖ $C_{CF\ out+}$ (fF)	61.71 ‖ 14.75
$R_{CF\ out-}$ (kΩ) ‖ $C_{CF\ out-}$ (fF)	61.71 ‖ 20.94

TABLE II. Parameters of $C_{0.75}$ and $L_{0.75}$ Emulators in Fig. 2. (Note: # in 30 kHz - 30 MHz; ‡ in 130 kHz - 2.5 MHz Ranges)

Component values (kΩ) / (pF)										
R_0	R_1	R_2	R_3	R_4	R_5	C_1	C_2	C_3	C_4	C_5
51.1	3.48	0.261	0.909	13.3	0.01	130	51	82	240	91
Total resistance (kΩ) / capacitance (pF)										
69.06						594				
Spread of resistance / capacitance										
5 110						4.71				
***C_γ*: Order (–) / phase (degree) / pseudo-capacitance (nF·sec$^{\gamma-1}$)**										
0.75 / –67.5 / 12										
***C_γ*: Phase angle deviation# (degree) / relative error# (%)**										
±0.9 / –1.35 → 0.6										
***L_γ*: Order (–) / phase (degree) / pseudo-inductance (mH·sec$^{\gamma-1}$)**										
0.75 / 67.5 / 17.3										
***L_γ*: Phase angle deviation‡ (degree) / relative error‡ (%)**										
±5 / 3.7 → 8.7										

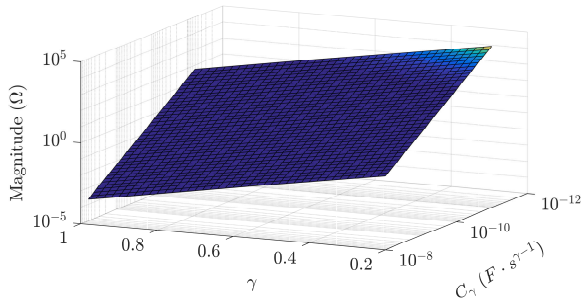


Fig. 4. Effect of C_γ vs. γ on FoL magnitude.

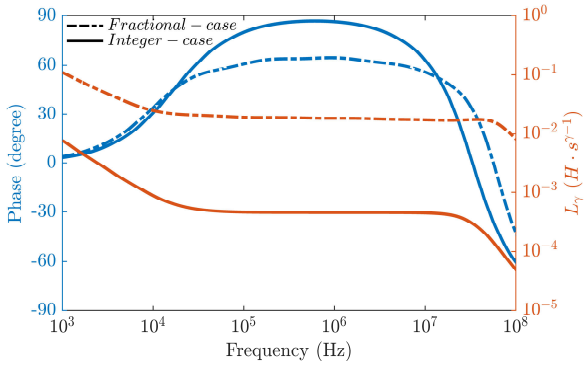


Fig. 5. Phase (left) and (pseudo)-inductance (right) responses of proposed 0.75 and integer-order CMOS inductance simulator.

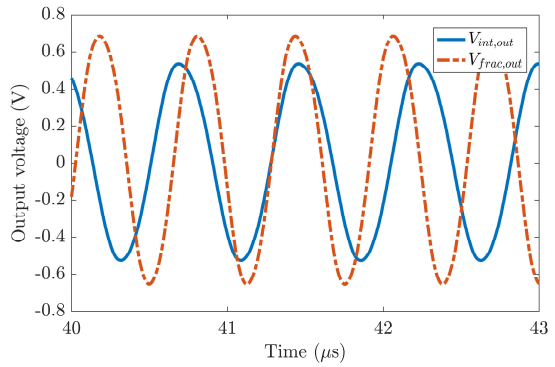


Fig. 6. Simulated output voltage waveforms of the proposed 2.75th and 3rd-order Colpitts oscillator.

order Colpitts oscillator were designed with CMOS transconductance given in Table I and capacitor values were selected as $C_1 = C_2 = 61$ pF. The calculated oscillation start-up condition is $R = 28.13$ kΩ and the FO is $f_{0\_theor\_fract} = 1.3$ MHz, while the simulated CO is $R = 30$ kΩ and FO is 1.58 MHz. On the other hand, the CO is 1.8 kΩ and FO is 1.26 MHz in integer-order case. The steady-state output voltage waveforms of both cases are depicted in Fig. 6. For the output the generated peak-to-peak value is 1.34 V and 1.06 V for 2.75th and 3rd-order, respectively, while the total harmonic distortion (THD) at the outputs are about 4.1% and 5.3% for the fractional and integer cases, respectively.

V. Conclusion

In this paper a fractional-order Colpitts oscillator design using a 0.75-order compact CMOS FoL simulator is presented. The C_γ with 12 nF·s$^{-0.25}$ value was emulated via 5th-order Foster II RC network and values optimized using MLSQ method. The resulted pseudo-inductance value of the proposed FoL is $L_\gamma = 18.4$ mH·s$^{-0.25}$ and its behavior and performance in oscillator was verified using SPICE simulations. Future work will be focused on experimental verification of the oscillator.

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